IN THE SPECIFICATION:

Please amend paragraph number **[0001]** as follows:

[0001] This application is a divisional of application Serial No. 09/389,316, filed September 2, 1999, ~~pending.~~ now U.S. Patent 6,295,730, issued October 2, 2001.

Please amend paragraph number **[0008]** as follows:

[0008] Yet another technique has been developed that uses a method for forming solder balls on a semiconductor plate having apertures. One such technique is described in United States Patent 5,643,831, entitled "Process for Forming Solder Balls on a Plate Having Apertures Using Solder Paste and Transferring the Solder Ball to Semiconductor Device," issued July 1, 1997 ("the '831 Patent"). The '831 Patent discloses a method for fabricating a semiconductor device using a solder ~~ball-forming~~ ball-forming plate having cavities. Solder paste is placed in the cavities using a solder paste application, such as a squeegee. Once the cavities are filled with solder paste, the solder ~~ball-forming~~ ball-forming plate is heated to form solder balls in the cavities while the plate is in an inclined position. The solder balls are then transferred from the plate to a semiconductor chip.

Please amend paragraph number **[0010]** as follows:

[0010] Yet another example of using a solder ball-forming plate is disclosed in United States Patent 5,607,099, entitled "Solder Bump Transfer Device for Flip-Chip Integrated Circuit Devices," issued March 4, 1997 ("the '099 Patent"). The '099 Patent discloses a carrier device that has cavities formed in its surface for receiving and retaining solder material. The solder material can then be transferred to a flip-chip as solder bumps. The cavities are located on the surface of the carrier device such that the location of the solder material corresponds to the desired solder bump locations on the flip-chip when the carrier device is placed in alignment with the ~~flip chip.~~ flip-chip. The size of the cavities can be controlled in order to deliver a precise quantity of solder material to the flip-chip. Further, in the '099 Patent, the apertures are fabricated so that they have a width of about 300 μm at the surface of the die and a width of

about 125 μm at its base surface. Meanwhile, in the '831 Patent, the rhombus-shaped cavities are ~~design~~ designed to produce a ball size of about 100 μm in diameter. Unfortunately, both of these structures cannot yet produce a ball size for a solder ball that approaches the dimensions currently required in placing a semiconductor chip upon a carrier substrate using the flip-chip technology. Additionally, the solder ball-forming cavities are limited in shape.

Please amend paragraph number **[0014]** as follows:

[0014] FIGs. 1A-D illustrate a cross-sectional view of steps used in forming ~~solder-receiving~~ solder-receiving holes and channels in a substrate mold according to the present invention;

Please amend paragraph number **[0027]** as follows:

[0027] FIG. 14 depicts the second substrate of FIG. 13 having the rectangularly shaped solder paste thereon after ~~the substrate mold has~~ having been removed from the substrate of the third embodiment of the invention by the heating thereof;

Please amend paragraph number **[0032]** as follows:

[0032] Illustrated in drawing FIGS. 1A-1D is a method for fabricating the semiconductor substrate to form metal bumps or metal traces, or both, on the surface of a secondary substrate. A semiconductor substrate, typically a flat planar substrate having a flat planar upper surface, a flat planar lower surface, and a plurality of planar sides forming the periphery of the substrate, is selected to serve as a bump-forming substrate mold 10. The semiconductor substrate may be of any desired size and geometric shape suitable for use with an associated semiconductor device. The semiconductor substrate is selected from a semiconductor base material such as silicon, gallium arsenide, silicon on insulator, which may include silicon on glass or sapphire, or other well-known semiconductor substrate materials, as well as other similar types of materials, which are capable of being precisely micromachined and having a coefficient of thermal expansion (CTE) similar to that of the semiconductor materials. In this particular

application, it is preferred that a silicon substrate is used for substrate mold 10, although any of the other base materials may be freely substituted therefor. The silicon substrate is aligned such that the flat, planar ~~substrate~~ upper surface 12 of substrate mold 10 defines the <100> plane of the substrate mold 10 which mates with a semiconductor device (not shown). As is shown in drawing Fig. 1A, the flat, planar ~~substrate~~ upper surface 12 of substrate mold 10 has a first protective mask layer 14 located thereon. The first protective mask layer 14 serves to protect the surface of substrate mold 10 when a subsequent etch ~~schedule~~ is performed to make the cavities or apertures in the flat, planar ~~substrate~~ upper surface 12. ~~Mask~~ First protective mask layer 14 may be selected from particular etch-resistant materials such as nitride, oxide, or a hardened polymer spin-on mask. Substrate mold 10 typically has a thickness of about 25 to 28 mils.

Please amend paragraph number **[0033]** as follows:

[0033] Next, in drawing FIG. 1B, a photoresist 16 is applied over the surface of first protective mask layer 14 and then exposed through a mask to define openings exposing the selected cavity locations to be formed in the flat, planar ~~substrate~~ upper surface 12. Then, as shown in FIG. 1C, a sufficient amount of semiconductor material is removed by an anisotropic etching from the exposed portion of the flat, planar ~~substrate~~ upper surface 12 after penetration of the exposed portion of first protective mask layer 14, thereby forming at least one cavity 18. Using an anisotropic etching process, the cavity 18 has walls sloped at 54° relative to the <100> plane of the substrate mold 10. The anisotropic etchant may be, for example, KOH, or other etchant materials well known to those skilled in the art. Further, if straight walls are desired, a dry etch using a plasma etch apparatus may be used to form cavity 18.

Please amend paragraph number **[0034]** as follows:

[0034] After the formation of cavity 18, first protective mask layer 14 is removed using a dry-etch process that is selective to removing first protective mask layer 14 only and not removing any of the underlying silicon either in the cavity 18 thus formed or on the flat, planar ~~substrate~~ upper surface 12 of substrate mold 10. For example, if first protective mask layer 14 is

silicon dioxide, a removal substance such as phosphoric acid may be used. After the removal of the first protective mask layer 14, a release layer 20 is formed over the entire flat, planar ~~substrate~~ upper surface 12 of substrate mold 10, particularly covering cavity 18. Release ~~material~~ layer 20 is selected from a material that is relatively nonwettable to metal solder. Such materials include silicon dioxide or silicon nitride, which can be applied using a chemical vapor deposition process. Other materials that are relatively nonwettable to metal solder may also be used, such as nonwettable polymers or the like. The ~~result in~~ resulting structure is depicted in drawing FIG. 1D.

Please amend paragraph number **[0035]** as follows:

[0035] Although drawing FIGS. 1A-D illustrate only a single cavity 18, it is intended that a plurality of cavities be formed in an array across substrate mold 10. An example of a solder ~~ball forming~~ ball-forming mold or substrate mold 10 that has such a plurality of cavities 18 is depicted in drawing FIG. 2. Release layer 20 (FIG. 1D) is applied and utilized to minimize the wetting of solder paste on the substrate mold 10 when the assembly is heated in order to transfer the solder onto the bumps of the secondary surface.

Please amend paragraph number **[0036]** as follows:

[0036] Solder paste is applied, as shown in drawing FIG. 3, by use of an applicator 22, such as a squeegee, that is passed across the surface of substrate mold 10, pressing a metal solder paste 24 into the plurality of cavities 18 and wiping the excess paste away. The metal solder paste 24 fills cavities 18, thus forming ~~frustroconically~~ frustoconically shaped solder bumps 26 (shown in FIGS. 3 and 4).

Please amend paragraph number **[0038]** as follows:

[0038] Once the metal solder paste 24 is applied ~~to the~~ to flat, planar ~~substrate~~ upper surface 12 of substrate mold 10, the entire assembly is heated to a temperature sufficient enough to slightly melt the metal solder paste 24 in order to begin the formation of the solder bumps 26

to be transferred. As shown in drawing FIG. 4, after this partially melted solder state has been reached, substrate mold 10 is inverted and applied to the surface of a carrier substrate 28, which may comprise a semiconductor device (die), wafer, or flexible substrate, such as a flex tape. The assembly of the substrate mold 10 and carrier substrate 28 is heated to ~~a sufficient~~ sufficiently high enough temperature to cause solder bumps 26 to slightly reflow and release from the release layer 20 formed on substrate mold 10. Substrate mold 10 is then removed and solder bumps 26 adhere to bond pads, terminal pads or other ~~conductive,~~ solder wettable conductive sites 30 on carrier substrate 28, as shown in drawing FIG. 5. Next, an additional reflow step may be performed that causes solder bumps 26 to form into approximately spherically shaped solder balls 32 attached to solder wettable conductive sites 30 as depicted in drawing FIG. 6.

Please amend paragraph number **[0040]** as follows:

[0040] Although it has been depicted how spherically shaped solder balls 32 or bumps ~~32 are~~ are formed in drawing FIG. 4, it is also possible to form metal traces using substrate mold 10. The same type of patterning and etch steps as described with respect to FIGS. 1A-1B would be followed, but would include a layout that would form metal traces or channels.

Please amend paragraph number **[0041]** as follows:

[0041] A solder mold system is depicted in drawing ~~FIG. 7~~ FIG. 7, which incorporates the substrate mold 10 shown in drawing FIGS. 1-6. The mold system includes solder applicator 22 for spreading metal solder paste 24 as dispensed by metal paste dispenser 52. Once the paste is sufficiently in place within the cavities 18, the substrate mold 10 is mated to a secondary substrate, as shown in drawing FIG. 4, and then placed in a low-temperature metal paste reflow oven 54 to melt the paste to a sufficient enough consistency to form self-supported bumps and has sufficient enough tackiness to wet the conductive gates on the carrier substrate 28.

Please amend paragraph number **[0042]** as follows:

[0042] Referring to drawing Fig. 8, an alternative embodiment of a substrate mold 40 of the present invention is illustrated. The substrate mold 40 is similar to the substrate mold 10 described hereinbefore as to construction and methods of construction except that the cavities 18 formed therein are hemispherically shaped. As illustrated, the first protective mask layer 14 used to form the plurality of cavities 18 is present on portions of the flat, planar upper surface 42 of the substrate mold 40. As with the substrate mold 10, the substrate mold 40 may include a release layer 20 to aid in the release of the solder paste contained within the hemispherical cavities 18.

Please amend paragraph number **[0043]** as follows:

[0043] Referring to drawing Fig. 9, once the metal solder paste 24 is applied to flat, planar upper surface 42 of substrate mold ~~40 as~~ 40, as described herein with respect to substrate mold 10 illustrated in drawing Fig. 3, the entire assembly of the substrate mold 40 and carrier substrate 28 having solder wettable conductive sites 30 or bond ~~pads 30~~ pads located thereon for the metal solder paste 24 to be applied is heated to a temperature sufficient enough to slightly melt the metal solder paste 24 in order to begin the formation of the solder bumps 26 to be transferred.

Please amend paragraph number **[0044]** as follows:

[0044] As shown in drawing FIG. 9, after this partially melted solder state has been reached, the assembly of the substrate mold 40 and the carrier substrate 28 is inverted so that the metal solder paste 24 in cavities 18 is applied to the solder wettable conductive sites 30 on the surface of the carrier substrate 28, which may comprise a semiconductor device (die), wafer, or flexible substrate, such as a flex tape. The assembly of the substrate mold 40 and carrier substrate 28 is heated to a sufficiently high enough temperature to cause solder bumps 26 to slightly reflow and release from the release layer 20 formed on substrate mold 40. Substrate mold 40 is then removed and solder bumps 26 adhere to the conductive sites, bond pads, terminal

pads or other ~~conductive,~~ solder wettable conductive sites 30 on carrier substrate 28, as shown in drawing FIG. 10. Next, an additional reflow step may be performed that causes solder bumps 26 to form into approximately spherically shaped solder balls 32 attached to solder wettable conductive sites 30 as depicted in drawing FIG. 11.

Please amend paragraph number **[0046]** as follows:

[0046] Referring to drawing Fig. 12, an alternative embodiment of a substrate mold 50 of the present invention is illustrated. The substrate mold 50 is similar to the substrate molds 10 and 40 described hereinbefore as to construction and methods of construction except that the cavities 18 formed therein are generally rectangular, or square shaped (shown in dashed lines). The first protective mask layer 14 used to form the plurality of cavities 18 present on portions of the flat, planar upper surface 42 of the substrate mold 50 is not illustrated. As with the substrate mold 10, the substrate mold 50 may include a release layer 20 to aid in the release of the solder paste contained within the hemispherical cavities 18. Referring to drawing Fig. 13, once the metal solder paste 24 is applied to flat, planar upper surface 42 of substrate mold ~~50 as~~ 50, as described herein with respect to substrate mold 10 illustrated in drawing Fig. 3, the entire assembly of the substrate mold 50 and carrier substrate 28 having solder wettable conductive sites 30 or bond ~~pads 30~~ pads located thereon for the metal solder paste 24 to be applied is heated to a temperature sufficiently high enough to slightly melt the metal solder paste 24 in order to begin the formation of the solder bumps to be transferred.

Please amend paragraph number **[0047]** as follows:

[0047] As shown in drawing FIG. 13, after this partially melted solder state has been reached, the assembly of the substrate mold 50 and the carrier substrate 28 is inverted so that the metal solder paste 24 is applied to the solder wettable conductive sites 30 on the surface of ~~the a~~ the carrier substrate 28, which may comprise a semiconductor device (die), wafer, or flexible substrate, such as a flex tape. The assembly of the substrate mold 50 and carrier substrate 28 is heated to a sufficiently high enough temperature to cause solder bumps 26 to slightly reflow and

release from the release layer 20 formed on substrate mold 50. Substrate mold 50 is then removed and solder bumps 26 adhere to the conductive sites, bond pads, terminal pads or other ~~conductive,~~ solder wettable conductive sites 30 on carrier substrate 28, as shown in drawing FIG. 14. Next, an additional reflow step may be performed that causes solder bumps 26 to form into approximately spherically shaped solder balls 32 attached to solder wettable conductive sites 30 as depicted in drawing FIG. 15.

Please amend paragraph number **[0049]** as follows:

[0049] Referring to drawing Fig. 16, another embodiment of the substrate mold 100 of the present invention is illustrated. The substrate mold 100 is similar to the substrate molds 10, 40, and 50 described hereinbefore. The substrate mold 100 includes cavities 18 having any desired shape as described herein in the flat, planar ~~substrate~~ upper surface 12 and includes electrical resistance heating strips 66 located on the bottom thereof for the heating of the substrate mold 100 with electrical conductor 68 connected thereto. The bottom surface of the substrate mold 100 includes a coating 62 thereon to electrically insulate the electrical resistance heating strips 66 from the substrate mold 100. The electrical resistance heating strips 66 may be of any desired geometrical configuration to cover the bottom surface of the substrate mold 100 to uniformly heat the mold 100 and the metal solder paste 24 located in the cavities 18 thereof. The electrical conductor 68 may be any desired shape and have any desired location for connection to the electrical resistance heating strips 66. The electrical conductor 68 is covered with an insulation layer 70 located thereover. In areas or portions of the bottom surface of the substrate mold 100 not having ~~a~~ an electrical resistance heating strip 66 located thereon, an insulative coating 64 of any suitable type is provided.

Please amend paragraph number **[0050]** as follows:

[0050] Referring to drawing Fig. 17, the substrate mold 100 is illustrated having metal solder paste 24 located in cavities 18 having release layer ~~coating~~ 20 therein. After the metal solder paste 24 is placed in the cavities 18, a carrier substrate 28 (see Fig. 4) is applied to the

substrate mold 100, the assembly of the substrate mold 100 and carrier substrate 28 inverted, and the electrical resistance heating strips 66 on the substrate mold 100 actuated to heat the metal solder paste 24 to transfer the same to the carrier substrate 28. After the metal solder paste 24 is transferred to the carrier substrate 28, the carrier substrate 28 is further heated to cause the solder paste to adhere to the solder wettable conductive sites 30 on the carrier substrate 28 to substantially form spherically shaped solder balls 32 thereon.

Please amend paragraph number **[0051]** as follows:

[0051] Referring to drawing Fig. 18, the electrical resistance heating strips 66 and electrical conductor 68 are illustrated. The electrical resistance heating strips 66 may be of any desired shape to substantially uniformly heat the substrate mold 100. Similarly, the electrical conductor 68 may be any desired shape to electrically connect to the electrical resistance heating strips 66. Further, any desired connector may be used to electrically connect the electrical conductor 68 to a source of electrical power.

Please amend paragraph number **[0052]** as follows:

[0052] Substrate molds 10, 40, 50 and 100 described herein are useful in forming contact bumps for many applications. One application is the formation of flexible connecting tape that requires bumps for interconnection of traces on the tape to a die or other element. The micromachining of substrate mold 10 provides a much more accurate means for placing the solder ~~ball shaped~~ ball-shaped bumps over the prior art methods of merely placing bumps on top of a screen and then having the screen place the bumps in a proper alignment. Further, the solder ~~ball shaped~~ ball-shaped bumps have a more uniform volume and shape as the cavity dimensions in the semiconductor mold provide a substantially precise control over the formation of the solder ~~ball shaped~~ ball-shaped bumps. By contrast, in the prior art, the uniformity of solder balls has always been a problem, especially at the smaller diameter dimensions that are now being used. Another application for the present invention is for the direct placement of the solder ~~ball shaped~~ ball-shaped bumps on a semiconductor device or die for attachment. Yet another

application includes placing the solder ~~ball shaped~~ ball-shaped bumps on a wafer-scale device for interconnection. This allows multiple devices placed on the same substrate to be interconnected using the precision of the solder ~~ball shaped~~ ball-shaped bumps. For example, the solder ~~ball shaped~~ ball-shaped bump application is useful in chip scale packages (CSP) or in fine ball grid array (FBGA) packages. The in situ electrical resistance heating strip allows for selecting which balls need to be transferred by selectively heating only those electrical resistance heating strips 66.

Please amend paragraph number **[0053]** as follows:

[0053] The applications of providing interconnect and bump contacts are numerous. For example, the metal trace interconnect and the bump contact may be used in any type of semiconductor device such as a memory storage device. These memory storage devices can range from read-only memory (ROM) and random access memory (RAM) to exotic types of ~~memory~~ memory, such as video memory and the memory used in computer systems. Additionally, the application of this metal trace interconnect and bump contact structure can be utilized in ~~micro processor~~ micro-processor packages that are used in computer systems as well as in other types of systems, and other types of single processing devices and support chips normally used in electronic devices. These electronic devices range from cellular phones to microwave systems, to automobiles and even to programmable wrist watches.